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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/065,202	09/25/2002	Thomas R. Bednar	BUR920020057	8155
28211	7590	12/23/2003	EXAMINER	
FREDERICK W. GIBB, III MCGINN & GIBB, PLLC 2568-A RIVA ROAD SUITE 304 ANNAPOLIS, MD 21401			DIMYAN, MAGID Y	
			ART UNIT	PAPER NUMBER
			2825	
DATE MAILED: 12/23/2003				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.		Applicant(s)	
	10/065,202		BEDNAR ET AL	
	Examiner		Art Unit	
	Magid Y Dimyan		2825 <i>AW</i>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 September 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-9,11-15,17-21,23-27 and 29-32 is/are rejected.
- 7) ☒ Claim(s) 3,10,16,22 and 28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 25 September 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 - 2, 4 - 9, 11 -15, 17 - 21, 23 - 27 and 29 - 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Morgan (U.S. Patent No. 6,083,271).

3. Referring to claim 1, Morgan cites a method of designing an IC that includes: supplying a chip design (Fig. 3, block 20); partitioning the elements in the design and creating voltage domains (i.e., islands) according to voltage requirements (Fig. 3, blocks 30, 40 and 50; column 2, lines 47 – 64); assessing and massaging the layout floorplanning and partitioning (column 3, lines 34 – 55; column 4, lines 29 – 62); and outputting a voltage island specification list (Figs. 3(A) – 3(D)). Thus, Morgan recites all the limitations claimed herein.

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4. As for claims 2, 4 and 5, see (3) above, as well as column 6, lines 41 – 63, which disclose how elements in the design are partitioned, with the same limitations as claimed herein.

5. Referring to claims 6, 7 and 21, see (3) and (4) above, as well as column 2, line 22 to column 3, line 8, which teach how power management of the overall chip design affects the partitioning of the layout, and the selection of the power domains, as claimed herein.

6. As for claim 27, see (5) above, as well as Figs 3A - 3D which recite the same limitations as claimed herein.

7. Claims 8 and 15 have the same limitations as claim 1, and thus the same rejections apply.

8. Claim 9 has the same limitations as claim 2, and therefore the same rejections apply.

9. Claims 11, 17, 23 and 29 have the same limitations as claim 4, and thus the same rejections apply.

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10. Claims 12, 18, 24 and 30 have the same limitations as claim 5, and thus the same rejections apply.

11. Claims 13, 19, 25 and 31 have the same limitations as claim 6, and therefore the same rejections apply.

12. Claims 14, 20, 26 and 32 have the same limitations as claim 7, and therefore the same rejections apply.

Allowable Subject Matter

13. Claims 3, 10, 16, 22 and 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: these claims pertain to the assessing of element waveforms, in the layout partitioning phase, to identify the timing of periods when these elements can be disconnected from a power supply. Prior art does not teach these limitations.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pub. No. US 2003/0079192 to Cheong et al discloses a method for generating a partitioned IC layout based on a netlist design in which a trial layout that only satisfies the various spatial, power, and other constraints (but not the timing constraints) is quickly produced; and acts as a basis for estimating sizes and floorplanning.

Pub. No. US 2003/0084416 to Dai et al cites a scalable partitioning IC layout system that initially modifies a netlist describing an IC as a hierarchy of circuit modules to combine clusters of cells forming selected modules so that they form a smaller number of larger cells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (703) 308-1354. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (703) 308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Magid Y Dimyan

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Examiner
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myd
December 16, 2003

A handwritten signature in black ink, appearing to read 'LMG', with a stylized, wavy line extending from the end.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER